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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,282	12/15/2000	Hideyuki Aoki	T&A-104	8133

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EXAMINER	
CHASE, SHELLY A	
ART UNIT	**PAPER NUMBER**
2133	7

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application No.	Applicant(s)	
	09/736,282	AOKI ET AL.	
	Examiner	Art Unit	
	Shelly A Chase	2133	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *45-49 and 53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44 and 50-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *45-49 and 53* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 to 44 and 50 to 52, drawn to testing memory devices, classified in class 714, subclass 718.

   II. Claims 45 to 49 and 53, drawn to manufacturing electronic devices, classified in class 700, subclass 95.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention group I has separate utility such as testing a memory device and dose not rely upon the method of manufacturing a computer for its patentability. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. John Mattingly on May 22, 2003 a provisional election was made without traverse to prosecute the invention of group I, claims 1 to 44 and 50 to 52. Affirmation of this election must be made by applicant in replying to this Office action. Claims 45 to 49 and 53 are withdrawn from further

consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Shelly A Chase
July 25, 2003

DETAILED ACTION

6. Claims 1 to 53 are presented for examination.

Election/Restrictions

7. Claims 45 to 49 and 53 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Priority

8. Receipt is acknowledged of papers submitted under 35 U.S.C. 119, which papers have been placed of record in the file.

Information Disclosure Statement

9. The references listed in the information disclosure statement submitted on 12-15-2000 have been considered by examiner (see attached PTO-1449).

Specification

10. The abstract of the disclosure is objected to because acronyms must be defined at their first usage in the specification, this objection applies to "PFBs" recited on line 7. Correction is required. See MPEP § 608.01(b).

Claim Objections

11. Claims 1 to 44 and 50 to 52 are objected to because of the following informalities: the claims are replete with typographically errors.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 2, 4,12, 14, 20, 22 to 23, 34, 41 and 52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, recites the limitation "said signals" recited on line 4. There is insufficient antecedent basis for this limitation in the claim.

Claims 4,12, 20, 23, 34, and 41, recites the limitation "adapted to check" recited on line 3. The functional limitation creates a vague and indefinite claim.

Claim 14, recites the limitation "to the memory" recited on line 5, this limitation is indefinite. The examiner is unclear as to the association of the memory in the claim.

Claim 22, recites the limitation "the memory mounted on said" recited on lines 2-3, this limitation is indefinite. The examiner is unclear as to the association of the memory in the claim.

Claim 52, recites the limitation "adapted to supply" recited on line 8. The functional limitation creates a vague and indefinite claim.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

15. Claims **14** to **16, 18, 20** to **22, 36** to **39, 41** to **44, 50** and **52** are rejected under 35 U.S.C. 102(e) as being anticipated by Le Blanc et al. (USP 6055653).

Claims **14 36** and **52**:

LeBlanc discloses a gangSIMM memory testing system [200], comprising: a gangSIMM Printed Wiring Assembly (PWA) [201] that is inserted into the testing system (see fig. 2A and col. 3, lines 60 to 65), ("a socket to be3 mounted with a memory device to be tested"); a test suite [209] providing test data (see col. 4, lines 40 to 45) interpreted as "a terminal supplied from a data processing unit mounted with a memory with signals...", and a comparator logic comparing the output from the SIMM's and the

signal output form the gold SIMM (see col. 6, lines 35 to 66), interpreted as "a control section for determining relationship between the output signals from said socket and the output signals from said memory."

As per claim **15**, LeBlanc discloses a customer replaceable unit (CR) computer system [208] including a CPU board [104] that includes SIMM slot [146] (see fig. 2a), ("first board") and gangSIMM PWA 201 inserting into slot [146] ("second board") wherein gangSIMM PWA [201] includes multiple SIMM slots and the system include the insertion of four or eight gangSIMM PWA (See col. 4, lines 13 to 25).

As per claim **16**, LeBlanc discloses CPU board includes slots [146, 148, 150, & 152] (see col. 5, lines 14 to 20); interpreted as "the apparatus comprises a plurality of types of said first boards to accommodate said memory device to be tested.")

As per claims **18** and **39**, Leblanc teaches testing a plurality of SIMM in parallel (see col. 5, lines 55 to 65).

As per claims **19** and **40**, Leblanc teaches an edge connector [320] providing communication from the processor through bus [105] (see col. 5, lines 51 to 57); interpreted as said data processing unit is coupled to said memory and comprise a control connector for controlling an operation of said memory.

As per claims **20** and **41**, LeBlanc discloses determining whether the gold and test data are equal (see col. 9, lines 48 to 52), interpreted as "said control circuit is adapted to check said signals for agreement/disagreement.

As per claims **21 and 42**, Leblanc discloses testing according to an address, data, output enable ("control signal") and timing (see fig. 6 and col. 10, lines 38 to 65).

As per claim **22**, LeBlanc discloses gangSIMM PWA includes buses [412, 414 and 416] for communicating addresses, data and control signals between gold SIMM and the plurality of test SIMM (see col. 5, lines 61 to 67), interpreted as "a substrate for taking out signals from the memory mounted on said data processing unit and supplying theme to said terminal".

As per claim **37**, Leblanc teaches a test suite supplying test data to a gold SIMM ("first memory device") and to a plurality of test SIMM ("second memory device") (see col. 4, lines 13 to 25).

As per claim **38**, Leblanc teaches testing a gold SIMM and a plurality if test SIMM (see col. 4, lines 13 to 25).

As per claim **43**, Leblanc discloses a gangSIMM test suite located on CPU board providing test data (see col. 4, lines 40 to 48); interpreted as " said apparatus for testing a memory module is adapted to define a test unit on said board".

As per claim **44**, Leblanc discloses testing one or several SIMM mounted on the gangSIMM PWA (see col. 4, lines 50 to 60).

Claim **50**:

LeBlanc discloses a gangSIMM memory testing system [200], including a gangSIMM Printed Wiring Assembly (PWA) [201] that is inserted into the testing system (see fig. 2A and col. 3, lines 60 to 65), comprising a gold SIMM [316] mounted on gangSIMM PWA [201] supplying test data to a plurality of SIMM (see col. 5, lines 51 to 65), interpreted as "a step of supplying said memory devices to be tested with signals to

be supplied said DIMM", and a comparator logic comparing the output from the SIMM's and the signal output form the gold SIMM (see col. 6, lines 35 to 66).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims **1** to **13**, **31** and **51** are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al. (USP 6499121 B1) in view of Momohara (USP 6094733).

Claims **1** and **9**:

Roy substantially teaches the claimed invention. Roy teaches a system for testing a number of integrated circuit (IC) devices under test (DUT) that are part of a wafer, the system comprising: a semiconductor device having a memory portion (see fig. 2 and col. 3, lines 46 to 50), a N channel tester [108] having a test program [206] supplying test data to the DUTs (see col. 3, lines 53 to 60), and interface circuitry [226] including sub-circuits [216a, 216b,...] for comparing expected data from the test program with data read from the respective DUT's (see col. 4, lines 6 to 31). Roy does not specifically teach the data processing unit have a first memory mounted on it; however, Momohara in an analogous art teaches a method for testing semiconductor memory devices wherein a memory testing unit [100] includes a main memory [103] that

stores the test program to test the semiconductor memory device (see col. 6, lines 27 to 35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the tester of Roy to include a memory as taught by Momohara. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to ensure the tester includes a storage device for storing instructions and test data to effectively test a semiconductor device.

As per claims **2** and **10**, Roy teaches the wafer includes a plurality of DUT (see fig. 2) and test data are applied simultaneously to the plurality of DUT's (see col. 5, lines 5 to 26).

As per claims **3** and **11**, Roy teaches a system controller [104] connected to the tester for controlling the test operations of the DUT; however fail to teach said data processing unit coupled to said first memory. Momohara teaches a CPU [102] connected to the main memory [103] (see fig. 8). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the test system of Roy to include a CPU connected to the main memory as taught by Momohara. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to ensure the controller controls the memory for effectively testing the semiconductor device.

As per claims **4** and **12**, Roy teaches the interface circuitry comparing the expected data and data read from each DUT checking for mismatch (see col. 6, lines 10 to 19).

As per claims **5** and **13**, Roy teaches the test program creates a test program, test address, and other control signals ("clock signals and control signals"), (see col. 3, lines 55 to 60).

As per claims **6** and **7**, Roy teaches the test program is passed to sub-circuits [216] and the sub-circuits pass the test data to their respective DUT's simultaneously (see col. 4, lines 6 to 19); interpreted as said signals supplied to said memory device to be tested is transferred by means of a pipeline system.

As per claim **8**, Roy teaches transferring test data, address data and control data to the sub-circuits and the sub-circuits transferring the data to their respective DUT's simultaneously (see col. 4, lines 48 et seq.); interpreted as said signal supplied by means of said pipeline system are distributed in a plurality of stages and supplied in parallel to said plurality of memory device to be tested.

Claims **31** and **51**:

Roy substantially teaches the claimed invention. Roy teaches a system for testing a number of integrated circuit (IC) devices under test (DUT) that are part of a wafer during manufacturing, the system comprising: a semiconductor device having a memory portion (see fig. 2 and col. 3, lines 46 to 50), a N channel tester [108] having a test program [206] supplying test data to the DUTs (see col. 3, lines 53 to 60), and interface circuitry [226] including sub-circuits [216a, 216b,...] for comparing expected

data from the test program with data read from the respective DUT's (see col. 4, lines 6 to 31). Roy does not specifically teach a step of forming the memory module by mounting on a substrate said memory device checked for the relationship in the preceding step; however, Momohara in an analogous art teaches a method for testing semiconductor memory devices wherein a memory testing unit [100] communicates with a test station [150] that includes a semiconductor chip [170] (see fig. 10) wherein a remedy determination process is performed after the semiconductor is check for an abnormal state to make a final determination of good or bad chips (see col. 8, lines 4 et seq.) and the throughput of each production line is increase (see col. 10, lines 29 to 39).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the tester of Roy to include a remedy step after the testing step indicates abnormal state as taught by Momohara since Momohara teaches remedying abnormal DUT's reduces testing cost and testing time. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a testing system for fast and efficient testing of semiconductor devices at a reduce cost.

18. Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. in view of Ito et al. (USP 5635832).

As per claim 17, LeBlanc does not specifically teach the memory device to be tested is a TSOP or a TCP; however, Ito in an analogous art teaches IC to be tested may be TSOP (thin small outline package) (see col. 2, lines 15 to 21). Therefore, it would

have been obvious to one having ordinary skill in the art at the time the invention was made to modify testing SIMM of LeBlanc to include testing TSOP as taught by Ito since, Ito teaches IC varies in form and all IC are tested. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a test system capable of testing various IC for their performance.

Conclusion

19. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for After Final communications)

(703) 746-7239, (for Official or Formal communications)

Or:

(703) 746-7240, (for Non-Official or Informal or "DRAFT" communications)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA.,

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

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Shelly A Chase
July 25, 2003